CLAIMS

What is claimed is:

1. An integrated circuit configured to capture an input signal to produce an output signal, said input signal being synchronized with a first clock signal, said output signal being synchronized with a second clock signal having a second frequency different from a first frequency associated with said first signal, comprising:

a first clock domain gating circuit having a first output terminal and a first input terminal, said first clock domain gating circuit being configured to be clocked by said first clock, said first input terminal being coupled to receive said input signal, said first clock domain gating circuit being configured to toggle a state of a signal on said first output terminal from one of a first state and a second state to the other of said first state and said second state every time a pulse is detected in said input signal, thereby producing a latched output at said first output terminal; and

a second clock domain gating circuit having a second output terminal and a second input terminal, said second clock domain circuit being clocked by said second clock, said second input terminal being coupled to said first output terminal to receive said latched output, said second clock domain gating circuit being configured to produce a pulse on said output signal at said second output terminal, said pulse on said output signal having a duration at least as long as a period of said second clock every time a state of said latched output changes.

2. The integrated circuit of claim 1 wherein said first clock domain gating circuit includes a first D flip-flop, said first input terminal being coupled to an ENABLE input of said first D flip-flop, said first output terminal being coupled to a first output terminal of said first D flip-flop, said first D flip-flop further includes a first complementary output terminal and a first data input terminal, said first complementary output terminal being coupled to said first data input terminal.

3. The integrated circuit of claim 2 wherein said second clock domain gating circuit includes a plurality of cascaded D flip-flops and an XOR gate, wherein said second input terminal representing a data input terminal of one of said plurality of

cascaded D flip-flops, an output of a next-to-last cascaded D flip-flop plurality of cascaded D flip-flops being coupled to a first input of said XOR gate, an output of a last-cascaded D flip-flop of said plurality of cascaded D flip-flops to a second input of said XOR gate, wherein said second output terminal of said second clock domain gating circuit is coupled to an output terminal of said XOR gate.

4. The integrated circuit of claim 3 wherein said second frequency is slower than said first frequency.

5. The integrated circuit of claim 1 wherein said second clock domain gating circuit includes a plurality of cascaded D flip-flops and an XOR gate, wherein said second input terminal representing a data input terminal of one of said plurality of cascaded D flip-flops, an output of a next-to-last cascaded D flip-flop plurality of cascaded D flip-flops being coupled to a first input of said XOR gate, an output of a last-cascaded D flip-flop of said plurality of cascaded D flip-flops being coupled to a second input of said XOR gate, wherein said second output terminal of said second clock domain gating circuit is coupled to an output terminal of said XOR gate.

6. The integrated circuit of claim 1 wherein said second frequency is slower than said first frequency.

7. A method for forming an integrated circuit, said integrated circuit being configured to capture an input signal in order to produce an output signal, said input signal being synchronized with a first clock signal, said output signal being synchronized with a second clock signal having a second frequency different from a first frequency associated with said first signal, comprising:

providing a first clock domain gating circuit having first clock domain gating enable input, a first clock domain clock input, a first clock domain gating data input, a first clock domain gating output, and a first clock domain gating complementary output;

coupling said input signal to said first clock domain gating enable input of said first gating circuit;

coupling said first clock signal to said first clock domain gating clock input of said first clock domain gating circuit, thereby clocking said first clock domain gating circuit with said first clock signal;

coupling said first complementary output of said first clock domain gating circuit to said first clock domain gating data input of said first clock domain gating circuit, wherein said first clock domain gating circuit being configured to toggle a state of a signal on said first clock domain gating output from one of a first state and a second state to the other of said first state and said second state every time a pulse is detected in said input signal, thereby producing a latched output signal at said first clock domain gating output; and

providing a second clock domain gating circuit, said second clock domain gating circuit having a second clock domain gating input and a second clock domain gating output configured to output said output signal, said second clock domain gating circuit being clocked by said second clock signal; and

coupling said first clock domain gating output to said second clock domain gating circuit input.

8. The method of claim 7 wherein said second clock domain gating circuit is configured to produce a pulse on said output signal at said second clock domain gating output, said pulse on said output signal having a duration at least as long as a period of said second clock every time a state of said latched output signal changes.

9. The method of claim 8 wherein said first clock domain gating circuit includes a D flip-flop.

10. The method of claim 8 wherein said second clock domain gating circuit includes an XOR gate having an XOR output terminal coupled to said second clock domain gating output.

11. A method for forming an integrated circuit, said integrated circuit being configured to capture an input signal to produce an output signal, said input signal being synchronized with a first clock signal, said output signal being

synchronized with a second clock signal having a second frequency different from a first frequency associated with said first signal, comprising:

providing a first clock domain gating circuit comprising a first clock domain gating circuit output, said first clock domain gating circuit being clocked by said first clock signal, said first clock domain gating circuit being configured to receive said input signal and to toggle a state of said first clock domain gating circuit output upon detection of each pulse on said input signal, said first clock domain gating circuit also being configured to hold said state, after toggling, between said detection of said each pulse on said input signal;

providing a second clock domain gating circuit comprising a second clock domain gating circuit input and a second clock domain gating circuit output configured for outputting said output signal, said second clock domain gating circuit being clocked by said second clock signal; and

coupling said first clock domain gating circuit output to said second clock domain gating circuit input.

12. The method of claim 11 wherein said pulse on said input signal is an active high pulse.

13. The method of claim 11 wherein said pulse on said input signal is an active low pulse

14. The method of claim 13 wherein said first clock domain gating circuit is a first D flip-flop, said first clock domain gating circuit output being a first D flip-flop output.

15. The method of claim 14 wherein said first D flip-flop further comprises a first D flip-flop complementary output and a first D flip-flop data input, wherein said first D flip-flop complementary output is coupled to said first D flip-flop data input.

16. The method of claim 15 wherein said input signal is coupled to an enable input of said first D flip-flop.

17. The method of claim 16 wherein said second clock domain gating circuit comprises a plurality of cascaded D flip-flops and an XOR gate having a first XOR input, a second XOR input, and an XOR output, each of said plurality of cascaded D flip-flops being clocked by said second clock signal, an output of a last cascaded D flip-flop of said plurality of cascaded D-flip-flops being coupled to said first XOR input, an output of a next-to-last-cascaded D flip-flop of said plurality of cascaded D flip-flops being coupled to said second XOR input, said XOR output being coupled to said second clock domain gating circuit output.

18. The method of claim 17 wherein said first D flip-flop output is coupled to a data input of a first cascaded D flip-flop of said plurality of cascaded D flip-flops.

19. A method for forming an integrated circuit, said integrated circuit being configured to capture an input signal to produce an output signal, said input signal being synchronized with a first clock signal, said output signal being synchronized with a second clock signal having a second frequency different from a first frequency associated with said first signal, comprising:

providing a first clock domain gating circuit having a first output terminal and a first input terminal, said first clock domain gating circuit being configured to be clocked by said first clock, said first input terminal being coupled to receive said input signal, said first clock domain gating circuit being configured to toggle a state of a signal on said first output terminal from one of a first state and a second state to the other of said first state and said second state every time a pulse is detected in said input signal, thereby producing a latched output at said first output terminal; and

providing a second clock domain gating circuit having a second output terminal and a second input terminal, said second clock domain circuit being clocked by said second clock, said second input terminal being coupled to said first output terminal to receive said latched output, said second clock domain gating circuit being configured to produce a pulse on said output signal at said second output terminal, said pulse on said output signal having a duration at least as long as a period of said second clock every time a state of said latched output changes.

20. The method of claim 19 wherein said first clock domain gating circuit includes a first D flip-flop, said first input terminal being coupled to an ENABLE input of said first D flip-flop, said first output terminal being coupled to a first output terminal of said first D flip-flop, said first D flip-flop further includes a first complementary output terminal and a first data input terminal, said first complementary output terminal being coupled to said first data input terminal.

21. The method of claim 20 wherein said second clock domain gating circuit includes a plurality of cascaded D flip-flops and an XOR gate, wherein said second input terminal being coupled to a data input terminal of one of said plurality of cascaded D flip-flops, an output of a next-to-last cascaded D flip-flop plurality of cascaded D flip-flops being coupled to a first input of said XOR gate, an output of a last-cascaded D flip-flop of said plurality of cascaded D flip-flops being coupled to a second input of said XOR gate, wherein said second output terminal of said second clock domain gating circuit is coupled to an output terminal of said XOR gate.